

THE DESIGN AND DEVELOPMENT OF THE SMEX-*Lite* POWER SYSTEM

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**Abstract:**

This paper describes the design and development of a 250W orbit average electrical power system electronic Power Node and software for use in Low Earth Orbit missions. The mass of the Power Node is 3.6 Kg (8 lb.). The dimensions of the Power Node are 30cm X 26cm X 7.9cm (11in. X 10.25 in X 3.1 in.) The design was realized using software, Field Programmable Gate Array (FPGA) digital logic and surface mount technology. The design is generic enough to reduce the non-recurring engineering for different mission configurations. The Power Node charges one to five, low cost, 22-cell 4 AH D-cell battery packs independently. The battery charging algorithms are executed in the power software to reduce the mass and size of the power electronic.

The Power Node implements a peak-power tracking algorithm using an innovative hardware/software approach. The power software task is hosted on the spacecraft processor. The power software task generates a MIL-STD-1553 command packet to update the Power Node control settings. The settings for the battery voltage and current limits, as well as minimum solar array voltage used to implement peak power tracking are contained in this packet.

Several advanced topologies are used in the Power Node. These include synchronous rectification in the bus regulators, average current control in the battery chargers and quasi-resonant converters for the Field Effect Transistor (FET) transistor drive electronics. Lastly, the main bus regulator uses a feed-forward topology with the PWM implemented in an FPGA.

**Background**

During the system definition of SMEX-*Lite*<sup>1</sup> significant restrictions were placed on the size and mass of the Power Node. The restrictions imposed by SMEX-*Lite* required reductions in size and mass of 50% over previous SMEX power system electronics development. A comparison of the SMEX power electronic to the Power Node shows that the goals were achieved. The PWB area is reduced from 4258 cm<sup>2</sup> (660 in<sup>2</sup>) to 1567 cm<sup>2</sup> (243 in<sup>2</sup>) thus reducing the circuit board assemblies from 9 to 2. This translates to a weight savings of about 5.5Kg (12 lbs.), from 8.6 Kg (19 lbs.) to 3.6 Kg (8 lbs.) The old SMEX power system also had two enclosures while the Power Node is contained in one enclosure. The number of connections is also reduced from 344 for the old design to 175 for the Power Node. The battery chargers in the Power Node rely on computations performed by the power software. The algorithms

implemented for SMEX-*Lite* are extensions of what was developed and successfully flown on the SMEX FAST<sup>2</sup> mission. The FAST mission power system used part of a rad-hard 8085 spacecraft computer to implement power system safe modes and battery charging.

**Introduction:**

The Power Node implements a non-dissipative unregulated power system using two bus regulators and five battery chargers. A block diagram of the power system is shown in figure 1. The bus regulator is duty cycled to maintain the bus at 32 volts during the sun illuminated portion of the orbit. The five-battery regulators use solar array power not required by the spacecraft load to charge the batteries. The operation point on the solar array IV curve changes around the peak power point to provide required power. If the load increases past the solar array capability, the battery current

decreases to compensate. During eclipse the battery current from each battery flows through its charger to the input of the bus regulators, which are 100% duty cycled to transfer the battery voltage to the spacecraft bus.

The Power Node software task implements the Voltage/Temperature (V/T) charge equation, Ampere-Hour Integrator (AHI), Minimum Solar Array Voltage (MSAV) calculation and power system configuration and safe functions. Analog telemetry is gathered from the Power Node to perform the calculations at a 10Hz rate over the MIL-STD-1553.

The V/T charge equation determines what the battery voltage limit should be based upon the battery temperature. The AHI sums the battery current readings over a Charge/Discharge (C/D) cycle and works in conjunction with the C/D ratio to determine the batteries State-Of-Charge (SOC). The C/D ratio determines how additional charging must be performed to recharge because of losses in the charging process. The MSAV command is set to keep the solar array voltage above the peak power point.

The Power Node adjusts the battery charge current, if required, to maintain this minimum solar array voltage. This maximizes battery charge current for the current spacecraft load. The minimum voltage is selected based on solar array temperature, and age to insure the set point is above the peak power point.

After the calculations for the above functions are performed, the software generates a command packet to be transmitted to the Power Node via MIL-STD-1553. This packet contains the analog voltage settings for the above functions. This packet is updated and transmitted at a 10Hz rate.

The design of the Power Node is simple and its small size and low mass are achieved by using surface mount components and FPGA's. All digital logic is implemented in two FPGA chips.

The Power Node was designed to support the largest solar array that can be packaged in a Small Expendable Launch Vehicle (SELV) fairing. The Power Node can accept and convert 550W of solar array power from a solar array with a peak power voltage greater than 34 volts. The Power Node power bus has been tested at a steady state spacecraft power load of 340Watts. The efficiency at this load was 95%. Five low cost 22 D-cell NiCd battery packs is charged, by

five battery chargers in the Power Node. The cells within a battery pack must be matched quite closely, while matching of the battery packs themselves is less important. The five battery chargers have been tested at a steady state charging power of 320W. The efficiency at this load was 92%. The Power Node supports independent voltage and current commands for each battery, which allows the charging of many battery technologies. Some typical charge methodologies supported are current, voltage, voltage temperature, and amp-hour charging methods. The charge current of each battery charger is limited to 2.5 amps.

Since the power system is dependent on a functioning the flight processor, the following safe functions associated with the flight processor are executed in the Power Node hardware. If the Power Node does not receive commands from the spacecraft for 20 seconds the Power Node interface circuitry resets. If the condition persists for a programmable time interval, the Power Node will power down the spacecraft bus for 10 seconds to reset the computer. The Power Node will turn off the instrument power after a power cycle. The Power Node also accepts an external two wire differential command to power cycle the bus. For SMEX-Lite, this external command is generated from a hardware decoded ground command. The Power Node supports 7 switched loads including a 100W heater bus and a 175W instrument bus. Current monitoring is provided on all major power busses entering or exiting the Power Node. The Power Node is designed to survive the vibration environment specified in General Environmental Verification Specification-Small Expendable Launch Vehicle (GEVS)-SELV

### **Mechanical Configuration**

The SMEX-Lite Power Node houses all the electronics for the Power System. There are no shunt resistors. The only other components of the power system are the solar array assembly and the battery packs.

The dimensions of the Power Nodes are 30cm X 26cm X 7.9cm (11 in. X 10.25 in X 3.1 in.), and its mass is less than 7.94lb (3.60Kg). The Power Node contains two board assemblies. The boards are surface mount Printed Wiring Boards (PWB) glued to an aluminum core for structural support and heat sinking. The interface and

control PWBs are glued to a common heat sink. This assembly is called the interface/control assembly.

The Power Node also contains a power PWB, which is glued to another aluminum heat sink, which is also the base plate of the Power Node and radiator surface of the spacecraft structure. This assembly is called the power board assembly. The interface/control assembly is bolted to a machined cover. The cover attaches to the power board assembly. The Power Node has six external interface connectors mounted on standoffs that protrude through the cover. The battery power, solar array power, and bus interface connector are mounted to the power board assembly. The battery telemetry, MIL-STD-1553, and spacecraft interface connector are mounted to the control/interface assembly. Two interface connectors on the control/interface and power assemblies are used to electrically connect the assemblies. These connectors are mated as the cover is installed onto the base-plate. The mechanical structure holds the connectors together and view-ports in the cover allow the connector mating to be observed. Shims are used on the connector standoffs on the control/interface assembly to adjust the mating of these connectors.

The interface printed wiring board contains all interface logic associated with the MIL-STD-1553B interface including the interface chip, Random Access Memory (RAM), Read Only Memory (ROM), and interface FPGA. The assembly also includes a 16 bit Analog-to-Digital Converter (ADC) with multiplexer and associated telemetry amplifiers, as well as A 12 bit Digital-to-Analog Converter (DAC), which is de-multiplexed to 11 channels. A block diagram of the interface board is shown in figure 2. The control board contains all of the circuitry for controlling the battery and bus regulators including the FET command generation, battery PWM chips and associated analog controllers, the solar array voltage ADC's for bus regulator control and the bus over-voltage comparitors. A block diagram of the control board is shown in figure 3. The power board assembly includes power filters and the power stages for the bus and battery regulators. The board also includes the FET drivers, resistive current sensing elements for current sensing and the bus power switches. A block diagram of the power board is shown in figure 4.

## **Power System Software and Operations**

The power system is designed to be simple to operate and configure. The system is reset at initial power up. At that point energy is automatically transferred to the spacecraft essential loads. The spacecraft computer powers up and configures the Power Node based on the detected state of two battery-on line signals. With no Ground Support Equipment (GSE) present the signals default to the on-line state. The GSE has two switches which can command the signals to the off-line state. Once one command is in the on-line state the computer will bring the batteries on line. If at any time both battery on line signals indicate off line status the batteries will be taken off line and the software will enter ground test mode. Once the batteries are brought on line they can only be commanded off line by the ground based GSE.

The power software continually monitors the configuration of the Power Node. If the software detects a configuration error, it sends commands to reconfigure the Power Node to the correct state. The power software must configure the battery and bus regulators for eclipse or daylight operations. The Power Node and power software, monitor the solar array current telemetry point to make the day/night determination.

The power software continually computes the state of charge for each battery. Battery current and temperature data are read from the Power Node and used to update each battery state of charge at a 10 Hz rate. The software also uses the battery temperature information to compute a voltage limit based on temperature for each battery. The software if enabled to do so can reduce the battery current to a programmable trickle charge level when the battery reaches 100% state of charge. The power software is configured to charge the batteries using the voltage temperature method at initialization. Ground commands are required to enable the AHI trickle charge mode. The power software sends a packet to the Power Node, which contains five battery voltage limits, five battery current limits and one solar array voltage limit.

One can stop using a battery by setting its charge current to zero for the remainder of the mission. The battery charger will isolate the battery from the solar array bus if its voltage is lower than all

other batteries and the charger is disabled. This would allow a failed battery to be effectively disconnected from the system.

If at any time during ground operations the spacecraft computer drops off line or is taken off line for diagnostics, the laptop with Airborne Support Equipment (ASE) software, see figure 1, can request telemetry and send commands to the Power Node via the MIL-STD-1553. The ASE is used throughout the Power node development and test. It is used during Power node box level testing, spacecraft integration, and launch operations. The ASE interfaces to the ITOS system over a network connection and to the power node using MIL-STD-1553. The ASE is capable of initiating or monitoring the activity of the Power Node. The ASE also controls the solar array simulators used during all phases of testing.

The Power Node and spacecraft can be powered down at any time by taking the batteries off line, using the battery off line switches, and turning off the solar array simulators. The order of these operations is not important. Also, no state information is stored in the Power Node. The Power Node will be completely cleared on power up with the exception of the battery on line flip-flops, which are only reset if both external inputs indicate that the batteries should be off line.

#### **SMEX-Lite Power Node Digital Electronics**

The Power Node contains two radiation tolerant Field Programmable Gate Arrays (FPGAs) which implement all digital electronic functions. FPGA's are used to reduce the size and mass of the digital electronics, and to make the design flexible. Flexibility results from the ability to change the design programmed into the part while maintaining fixed pin assignments. Once the pin assignments are made, digital design and simulation can proceed concurrently with board layout and fabrication. Since it was impossible to define all the signals required between the FPGA's at the beginning of the design a generic bus was added to allow communications between the FPGA's. This allowed the design and simulation of the FPGA's to proceed while hardware was being built.

The communications interface is implemented in an Actel A1280A, 8,000 gate one time programmable FPGA. This FPGA is installed on the interface board. The FPGA design contains

the state machines and decoding logic necessary to receive and transmit commands using the MIL-STD-1553 data bus. In addition, it has the ADC circuitry for gathering telemetry. The telemetry is gathered at a 10Hz rate by a state machine in the FPGA and read by the spacecraft computer. The interface FPGA was developed using a combination of Very High Level Design Language (VHDL) code and schematics. The state machines are coded using VHDL for ease of design and modification. The schematic is used for the decoding and interconnecting of the state machines.

This FPGA interfaces to the UTMIC Summit chip, which is a 1553 protocol chip with built-in dual transceivers. The FPGA and the Summit chip communicate through shared SRAM. The arbitration of the SRAM is done in the FPGA. In addition to the FPGA, Summit and SRAM, PROM is used for initialization of the MIL-STD-1553 interface (set-up table locations in SRAM and initialize Summit). The FPGA also contains a state machine which controls a 12-bit DAC. This DAC is commanded by the computer over the MIL-STD-1553 and generates the analog commands for the battery chargers and the solar array voltage control. The FPGA also contains a state machine which generates the drive signals for the 200 kHz quasi-resonant AC converter on the interface board.

A second FPGA, an ACTEL A14100A performs all digital functions for the Power Node power supplies. This 10,000 gate, one time programmable, FPGA is installed on the control board. The FPGA contains 5 registers used for Power Node configuration. The registers allow FET transistors in either the battery chargers or bus regulator to be turned off. Also the battery chargers can be enabled or disabled using these registers. The control bypass of the bus regulator controller and battery charger for eclipse operations is controlled in these registers. A state machine in the FPGA autonomously disables the battery chargers on entry into eclipse, and removes the bypass of the bus and battery controllers during non-eclipse periods. The state machine bases its decisions on the solar array current value sent to the control board FPGA over the general communications bus from the FPGA on the interface board. The FPGA on the control board also sends telemetry back to the FPGA on the interface board using this general communications bus. The FPGA accepts the PWM signals from the battery

chargers and generates the FET transistor commands. It also contains the digital logic to control the switched loads.

The FPGA implements the Pulse Width Modulator (PWM) controller for the bus regulator. The FPGA determines the duty cycle required and generates the commands to the FET transistors in the bus regulator. The duty cycle is a function of the solar array voltage which is sensed by the FPGA using a timer circuit. The FPGA also implements a redundant over-voltage function by turning off the appropriate FET transistors when an over-voltage event is detected. The FPGA determines the duty cycle required by zeroing the voltage across a comparator and timing how long the capacitor, charging from the solar array bus, takes to reach a fixed voltage and trip a compactor. This time is checked to determine out-of-bound conditions and then is converted into a pulse width. Two ADC timer circuits are included in the Power Node. The FPGA changes which ADC circuit is used every power cycle. This allows correction of a catastrophic ADC failure. The PWM can be calibrated to increase or decrease the pulse width from the ground by programming an offset register in the FPGA. This allows errors induced by part tolerances or drift to be corrected. The PWM is very configurable.

The FPGA on the control board also implements a power cycle of the spacecraft bus if commanded by the Computation Hub or if a time-out of the MIL-STD-1553 bus occurs. The time-out is programmable from the ground. The power-cycle is performed to bring the spacecraft bus down to 0 volts and up to bus voltage gradually over a 20 milli-second to 36 milli-second period depending upon the initial solar array bus voltage. The duration of power down is set to 10 seconds.

### **Bus Regulators**

The SMEX-Lite Power Node has two bus regulator circuits. Each circuit is designed to deliver 340 watts continuous power. With both circuits operating the bus regulators can supply 340 Watts continuous and peak loads approaching 500 Watts. The bus regulator conditions the 34 to 60 volt solar array energy, or 21-33volt battery energy and delivers it to the spacecraft bus. The output voltage of the bus regulator is approximately 32 volts when driven with solar array energy and equal to the battery

voltage when operating driven with battery energy. A block diagram of the bus regulators is shown in figure 5. The controller for the bus regulator FET transistors is implemented in a FPGA. The following elements are included in the bus regulator: Redundant Solar array bus ADC, Redundant Class D synchronous regulators, Filters, FET drive circuitry, and a FPGA which controls the bus regulator. The duty cycle of the class D modulators are limited to the range of 50% to 95% for normal control. The controller can be bypassed, or locked in eclipse to allow the class D modulators to operate at 100% duty cycle. The control method used is a feed forward controller which monitors the solar array bus voltage and adjusts the PWM to output 32 volts. Over-voltage comparitors, when activated, disable the high side FET transistors to prevent bus over-voltage events. The synchronous regulators use surface mount SMD-2 and SMD-1 FET transistors, which are radiation hard. The capacitors used are ceramic stacks and high density wet tantalums, and the inductors are custom fabricated from pot cores.

The synchronous rectification allows energy to flow in both directions. If the spacecraft bus is driven higher than the bus regulator set point, the bus regulator will transfer energy from the spacecraft bus to the solar array bus. In SMEX Lite spacecraft this can only occur in two ways. The first is the discharge of the capacitors on the bus during a power cycle. The second is the reaction wheels placing energy on the bus because the bus voltage is commanded below the wheel motor back EMF potential. Both of these events can cause the solar array bus voltage to rise. If the solar array voltage rises above 64 volts, a shunt resistor is connected across the solar array bus until the bus voltage drops under 62 volts. The resistor is selected to dissipate the worst case power available from the wheels during the power cycle. The wheels for SMEX-Lite were designed with a feature which prevents them from placing power on the spacecraft bus if the bus voltage is less than 18 volts. This reduces the time the resistor is required to dissipate energy to about 40 msec. The two redundant synchronous regulators each operate at 50 kHz. The timing signals of one regulator are delayed by 10 microseconds to implement a 180-degree phase shift. Commands are available to disable the low side FET transistors for either supply, or the high side FET transistor for one supply.

### **Battery Supplies**

The SMEX-Lite Power Node contains 5 independent battery chargers. Each charger accepts 34-60 volts on its input and provides a controlled current output with voltage limit from 24 to 32.2 volts. The current limit can be commanded in the range 0-2.5 amps, and the voltage range can be commanded in the range 20-33 volts. The battery chargers are buck derived and include two n-channel FET transistors. One transistor is operated by the PWM via the FPGA and provides charge energy to the battery. The second FET is activated by the FPGA and controls the ability of the battery to deliver energy to the spacecraft. See the battery charger block diagram in figure 6.

A PWM chip is used to control the duty cycle for each battery charger. The independent oscillators in the five PWM chips are synchronized and phased to reduce peak current requirement on the EMI filters. In addition, the battery chargers operate synchronous to the bus regulators to reduce EMI and provide a consistent noise environment. The PWM chips accept a voltage PWM command from an analog control circuit which implements average current control methodology. This methodology monitors the output inductor current at high bandwidth inverts it and subtracts it from a reference level. The output of the controller is a ramp, which appears inverted with respect to the ramp in the PWM chip. The PWM ramp generator ramps up when the FET is closed. The controller ramp signal ramps down during the same period. When the two ramps cross, the FET is turned off. One major advantage of average current control is the inductor current ramp signal dominates all other linear poles. This allows the current loop control stabilization to be based on a two-pole plant and greatly simplifies the stability criterion. This reduced pole plant allows the current control closed loop bandwidth to approach 8 kHz while operating over a wide range of voltages and currents. The battery chargers also operate quite well on both sides of the continuous/discontinuous conduction boundary, which allows the inductance in the battery charger to be physically smaller.

Functionally, battery current remains at its set point until the battery voltage rises to the voltage limit. The battery voltage controller then reduces the current set point to maintain the battery voltage at its set point. The solar array

voltage control operates by reducing the current set point of all the batteries at once. Each battery charger has three command inputs, one for the current set point, one for the voltage set point, and one for the solar array voltage control. The current and voltage set point are derived from 12 bit DAC outputs. The single solar array voltage control circuit drives the third output of all battery chargers. The battery charger protects itself with battery over voltage and over current shutdown. During eclipse, the battery charger allows energy to pass from the battery to the solar array bus. A lock scheme similar to the bus regulator is used which allows the body diode of the battery charging FET to be shorted in eclipse once the battery voltages are matched.

### **FET drive circuit**

The Power Node has nine N-channel FET transistors which are used in PWM operations. Two transistors are in the high side of the bus regulators, two are in the low side of the bus regulators, and five are in the battery chargers. The FET drive circuits for all these FETs are identical, which reduced design time and complexity. The FET commands originate in the FPGA and are buffered in a 54AC244. The outputs of the buffer are connected to a transformer. Two inverted outputs of the transformer are combined with diodes to generate a command for the FET driver chip. The FET driver chip in turn drives the FET. The FET driver chip gets 10 volts from a transformer isolated power supply associated with each FET. The FET drive circuit was simulated exhaustively using PSPICE. The simulations included all aspects of the FET driver including the digital driver, transformer, surface mount ferrite beads, FET driver chip and the FET itself. The simulations allowed circuit values to be verified and the impedance of the ferrite beads and transformer windings to be optimized. The FET drive circuit is shown in figure 7.

### **Power Node Analog Modeling**

SPICE simulations were used to verify the operation of most circuits in the Power Node. The modeling effort was quite successful. Circuits usually worked at first application of power. In all cases but one, circuits that had problems did not match the simulation. In one

case, the circuit did not work and it was determined that the simulation showed the circuit problem. The problem was missed when the simulation data was reviewed. The simulations would have been more helpful if they could have been run using the netlist used for board layout. The tools did not easily support this capability and this weakness led to all but one of the errors found at board level testing. The other major limitation of our tools was the model complexity, which could be executed. The initial goal was to simulate the operation of the entire Power Node using PSPICE in one large simulation. A model of an entire battery charger was built with no simplifications. The model had significant numerical instability problems and often crashed the simulator. After this experience, individual simplified circuits were simulated. The following Power Node circuits were simulated: FET drive, Battery charger output, Bus regulator output, Bus power switches, Battery charge control, Solar array bus ADC timer, 200 kHz AC supply, LVPC linear regulator, battery on line command, and numerous telemetry circuits. A simplified overall model was also built to verify the overall performance of the control loops and was successfully executed. This model was used to tune the control parameters and allowed the system to function successfully at full power on the first attempt. The modeling effort added significant time to the schedule and slowed Power Node development but, it allowed measurements to be made which would have been impossible using scopes and current probes. These measurements allowed the circuits to be optimized and tested more exhaustively than would have been possible with breadboards. Also the debugging of problems with breadboard and proto-flight boards were significantly simplified by comparing the performance of the hardware with the simulation.

#### **Power bus interface and Low Voltage Power converter**

The SMEX Lite Power Node supports 7 power switches and 8 bus current monitors. All of the power switches are implemented with N-channel FETS. A high side driver chip operating from a bus plus 10 supply is used to drive the gate of the FETS. Resistors and redundant zeners protect the gates of the FETS against overvoltage. The configuration of the power switches is shown in figure 8.

The low voltage power converters used for the Power Node are high reliability commercially available power supplies. The LVPS subsystem accepts power from the bus regulator and from the solar array bus through a dissipation regulator. The dissipation regulator provides power to the Power Node during initial power up.

#### **Radiation**

The Power Node was designed to be "radiation tolerant". The phrase "radiation tolerant" in this paper means no latch-up at LET < 80MeV for SEL, total dose 15K rad (Si) and SEU LET 28MeV-cm<sup>2</sup>/mg for the critical modules and SEU LET ~8MeV-cm<sup>2</sup>/mg for non critical modules. It is important to note that there are now "rad-hard" FPGA parts becoming available which are pin for pin compatible with the currently used "radiation tolerant" ones. The phrase "rad-hard" in this paper means the following: no latch-up (LET>80MeV for SEL), total dose ~100K rad (Si)/sec and SEU LET ~30MeV-cm<sup>2</sup>/mg. Many of the components in the Power Node are "radiation hard". For example all FETS, RAM, PROM, MUX, ADC, DAC, and MIL-STD-1553 interface chips are "rad hard". Some of the op amps and other parts are soft for total dose and would require shielding for a high radiation orbit.

#### **Power Node Development**

The Power Node followed a standard protoflight development cycle. Simulations and breadboards were built for selective circuits. Boards are layed out, manufactured and assembled with a mix of flight and Engineering test unit parts. A full set of mechanical parts are designed and manufactured. A full set of custom magnetic components are fabricated and installed on the assembled cards. Card level tests are completed and Power Node integration and system testing is being performed. The Power Node qualification testing are performed after the SMEX-Lite proto-flight spacecraft is integrated. The qualification tests will include Thermal Vacuum, Vibration, and EMI.

The Power Node software was developed in the C++ computer language. The software is tested on a power PC computer using the VX-Works operating system using a MIL-STD-1553

simulator. The software is then executed on the flight R6000 processor in the flight environment with the Power Node.

The configuration used to test the Power Node at box level is shown in figure 9. The Integrated Test and Operations System (ITOS) is a Pentium based PC, which accepts commands and displays telemetry. In the box level setup, a laptop computer running the ASE software is the bus controller of the MIL-STD-1553 bus. The telemetry collected by the laptop is formatted by the laptop into packets identical to those generated by the flight processor. The packets are passed over the network to the ITOS system for display. The display formats used at box level are identical to those used at flight integration. Likewise, commands from the ITOS are passed over the network to the laptop which reformats the commands into MIL-STD-1553 packets and sends them to the Power Node. The commands used in this setup are identical to those which are used in flight integration. This allows commands, telemetry, and procedures to be debugged at box level before delivery to the spacecraft.

The test configuration for flight integration is shown in figure 1. The ITOS and laptop are identical to the units used at box level. The flight computer is the primary interface between the ITOS and the Power Node. The ASE laptops main function is to allow the operator to monitor the Power Node telemetry if the flight computer is not active and to command the solar array simulators. This allows the power system to be monitored and initialized without the ITOS system, a requirement for airborne launch operations.

A major development goal was to minimize the GSE required to support the Power Node testing. The ITOS system used at box level was already developed for use at spacecraft level. This reuse of the ITOS software for Power Node box testing saved time and money and also allowed the flight command and telemetry database to be tested at box level instead of spacecraft level. The battery simulator and the battery monitoring GSE were designed using the same hardware and software with different cables, to reduce cost.

The Power Node box level testing has been trouble free to this point. The cost savings realized by reusing the ITOS software, and flight

database at box level have been significant, and the test capabilities available using the ITOS system far exceed anything that could have been developed specifically for the Power Node.

### Conclusion

The development of the SMEX-Lite power system demonstrates the ability to build compact power systems for small spacecraft. The benefits of using modern digital computer and power techniques were also demonstrated. The Power Node is a first step for hybrid power systems for small low cost spacecraft. There are more capable FPGA chips, which would allow the digital electronics to operate from 3.3V. This would significantly reduce the power consumption of the Power Node, and increase its radiation tolerance at the same time. Higher density FPGA chips are also on the horizon. These chips will allow the battery charge function to be integrated into the FPGA, raising the density of the power system. The Radiation Hardened FET transistors used in this design are one generation old. The new units available in the same packages would increase the efficiency of the Power Node or increase its power handling capability. Currently, the resistance of the filters and output inductors are limiting the power handling capabilities of the Power Node. When the second Power Node is built, the resistance of these elements will be decreased. Also, future missions may allow the Power Node design to be adapted to charge one or two large batteries instead of the five D-cell packs. The Power Node will support low cost missions in LEO orbits and significantly reduce the cost of mission implementation. This is accomplished by reducing the amount of power hardware fabricated, and by using low cost, commercial battery technology.

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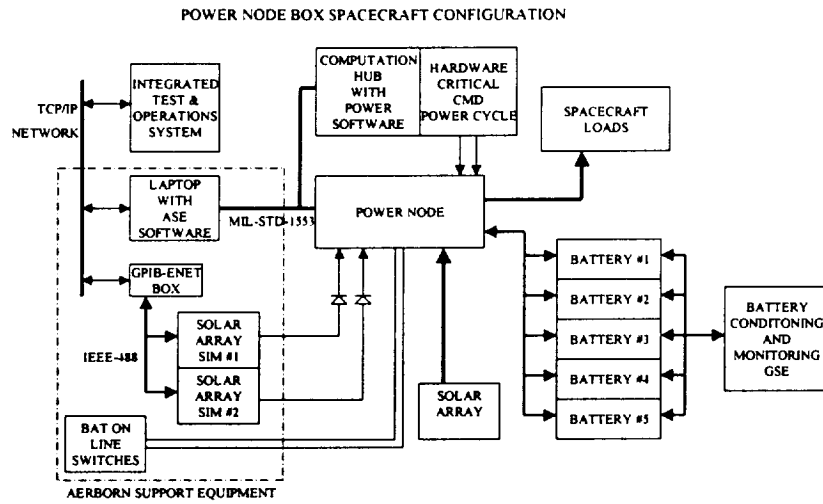


Figure 1: SMEX-Lite Power system configuration

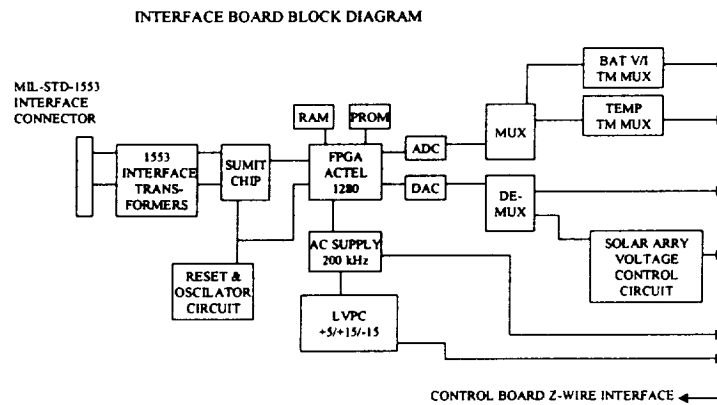


Figure 2:

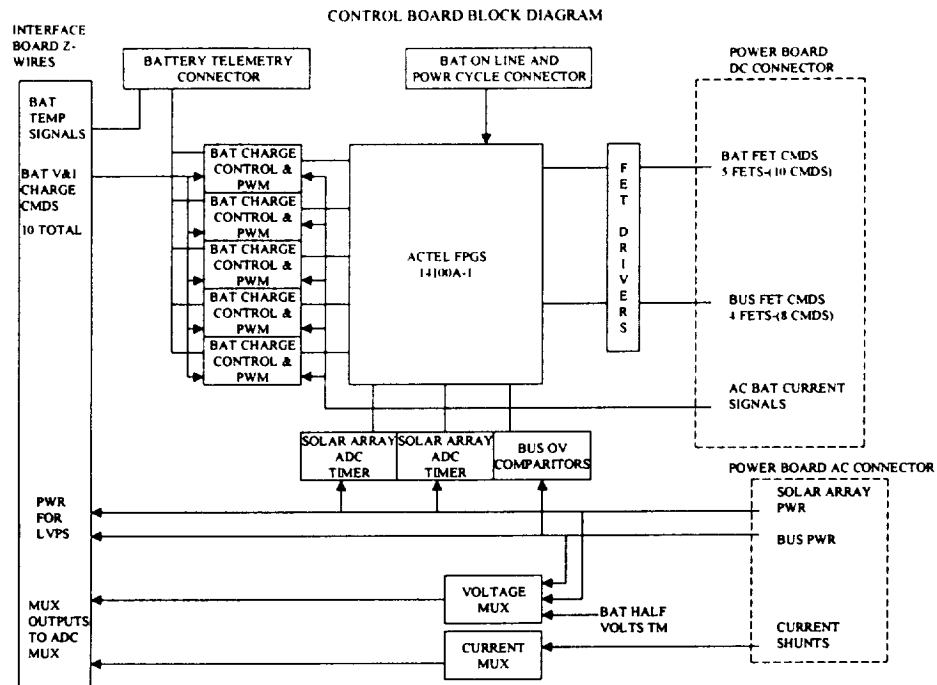


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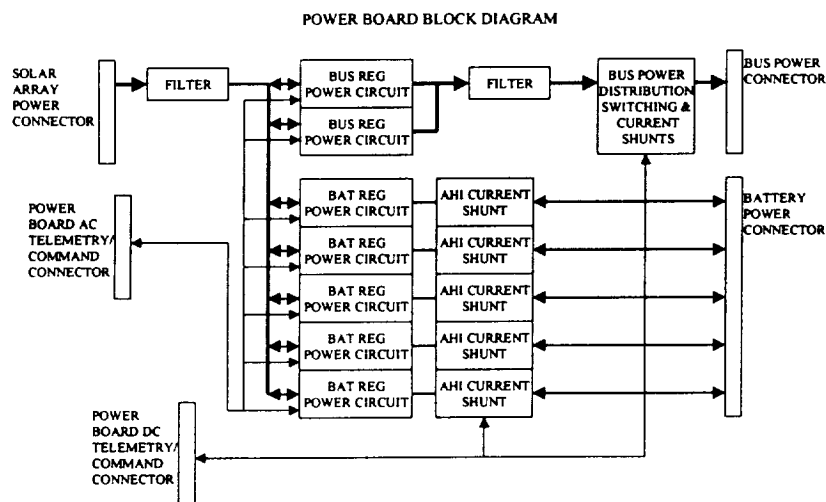


Figure 4:

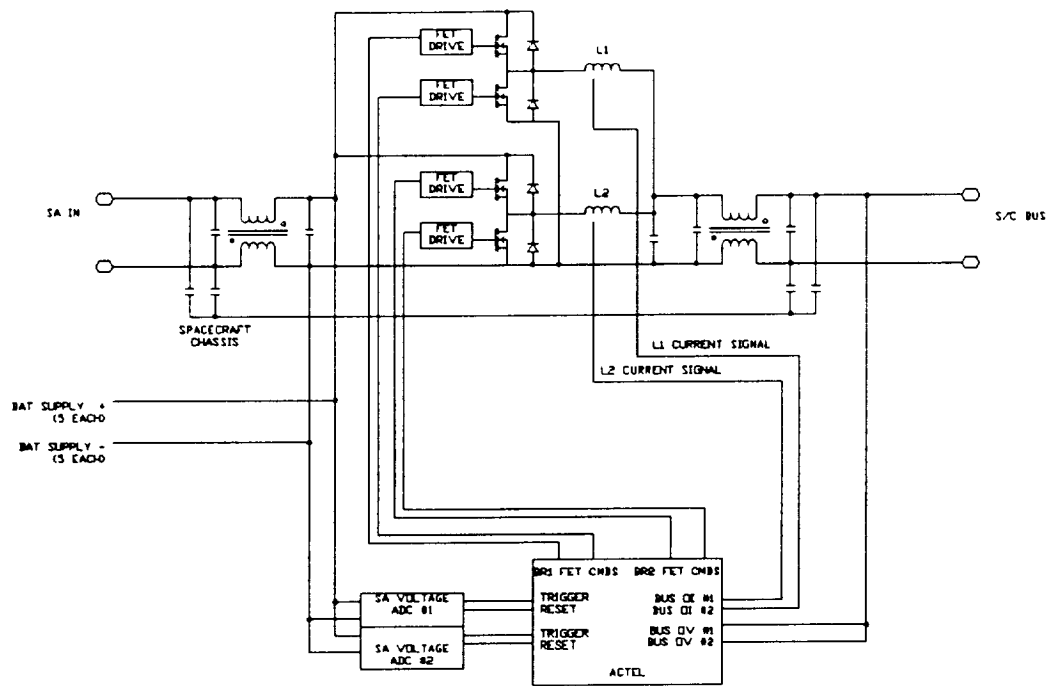


Figure 5: Bus Regulator Block Diagram

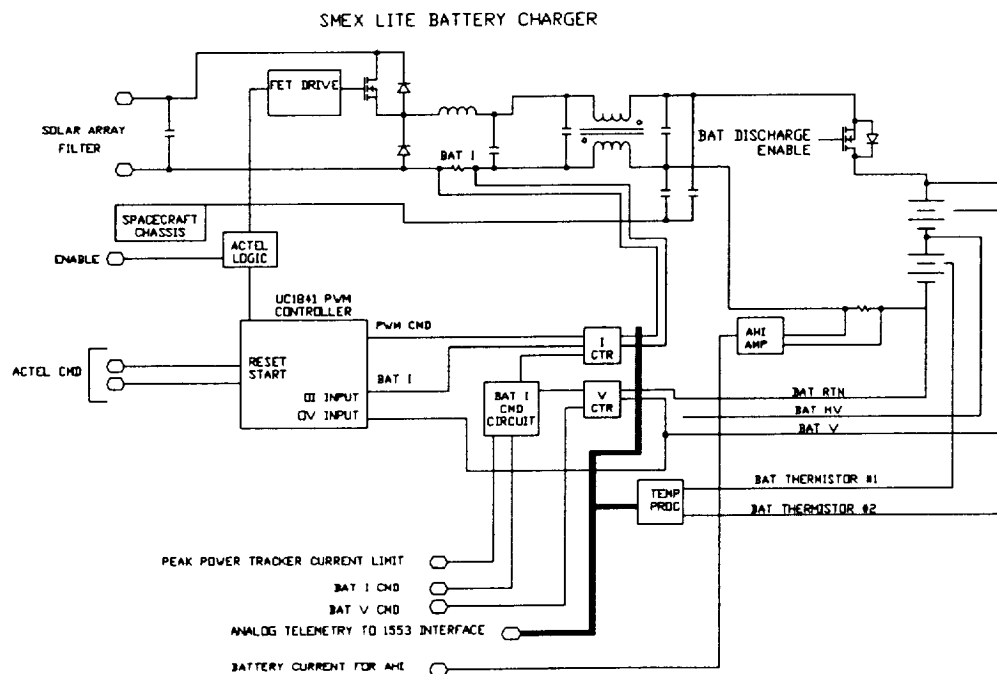


Figure 6: Battery Charger Block Diagram

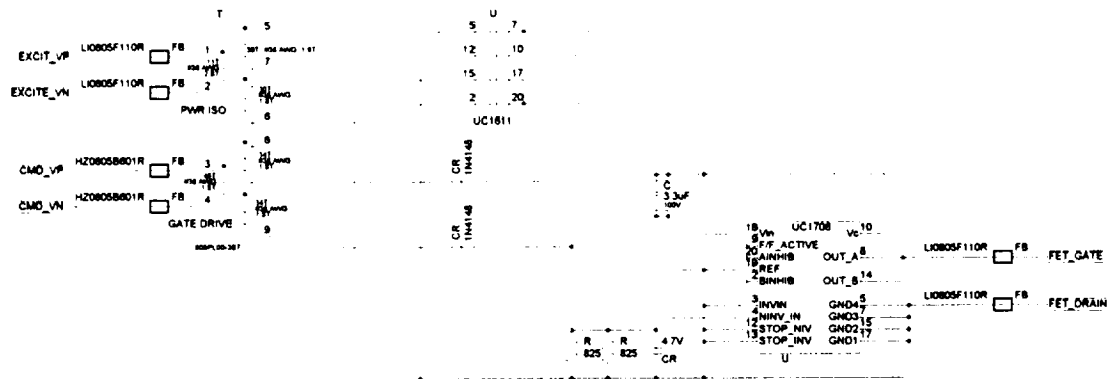


Figure 7: FET Transistor Drive Circuit

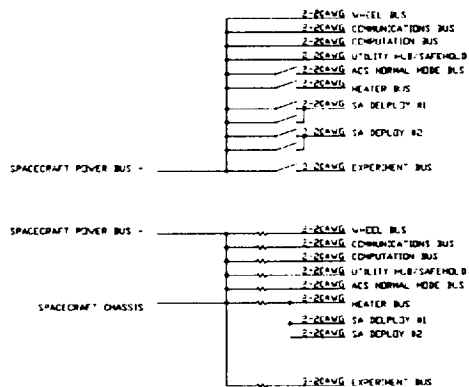


Figure 8:

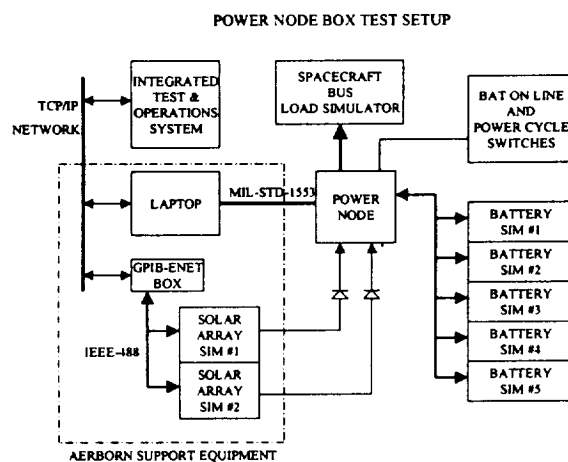


Figure 9:

References

<sup>1</sup> James G. Watzin. "SMEX-LITE – NASA's NEXT GENERATION SMALL EXPLORER"  
10th ~~Annual~~ Annual AIAA/USU Conference Sept 1996

<sup>2</sup> L. F. Dougherty, T. D. Gruner, J. Wilmot. "FAST AURORAL SNAPSHOT MISSION UNIQUE ELECTRONICS COMPLETE SPACECRAFT ELECTRONICS CONTAINED IN A SINGLE ENCLOSURE. 9<sup>th</sup> Annual AIAA/USU Conference on Small Satellites, 18-21 September 1995."